TC59S1616AFT-10, -12
TC59S1608AFT-10, -12
TC59S1604AFT-10, -12

PRELIMINARY

524,288 WORDS X 2 BANK X 16 BITS 1,048,576 WORDS X 2 BANK X 8 BITS 2,097,152 WORDS X 2 BANK X 4 BITS SYNCHRONOUS DRAM

Description

TC59S1616AFT is a CMOS synchronous dynamic random access memory organized as 524,288-words x2-banks x16-bits and TC59S1608AFT is a CMOS synchronous dynamic random access memory organized as 1,048,576-words x2-banks x8-bits andTC59S1604FT organized as 2,097,152 words x2-banks x4-bits. Fully synchronous operations are referenced at the positive edges of clock input and can transfer data up to 100M-words per second. These devices are controlled by commands setting. Each bank are kept active so that DRAM core sense amplifiers can be used as a cache. The refresh functions, either Auto Refresh or Self Refresh are easy to use. By having a programmable Mode register, the system can choose the most suitable modes to maximize its performance. These devices are ideal for main memory in applications such as workstations.

Features

- Single power supply of 3.3V±0.3V
- Up to 100MHz clock frequency
- Synchronous operation: All signals referenced to the positive edges of clock
- Architecture: Pipeline
- Organization
  - TC59S1616AFT
  - 524,288 words x 2 banks x 16 bits
  - TC59S1608AFT
  - 1,048,576 words x 2 banks x 8 bits
  - TC59S1604AFT
  - 2,097,152 words x 2 banks x 4 bits
- Programmable Mode register
- Auto Refresh and Self Refresh
- Burst Length: 1,2,4,8, Full page
- $\overline{\text{CAS}}$ Latency: 1,2,3
- Single Write Mode
- Burst Stop Function
- Byte Data Controlled by L-DQM, U-DQM (TC59S1616)
- 4K Refresh cycles/64ms
- Interface: LVTTL, Terminated LVTTL
- Package
  - TC59S1616AFT: TSOP44-P-400F
  - TC59S1608AFT: TSOP44-P-400F
  - TC59S1604AFT: TSOP44-P-400F

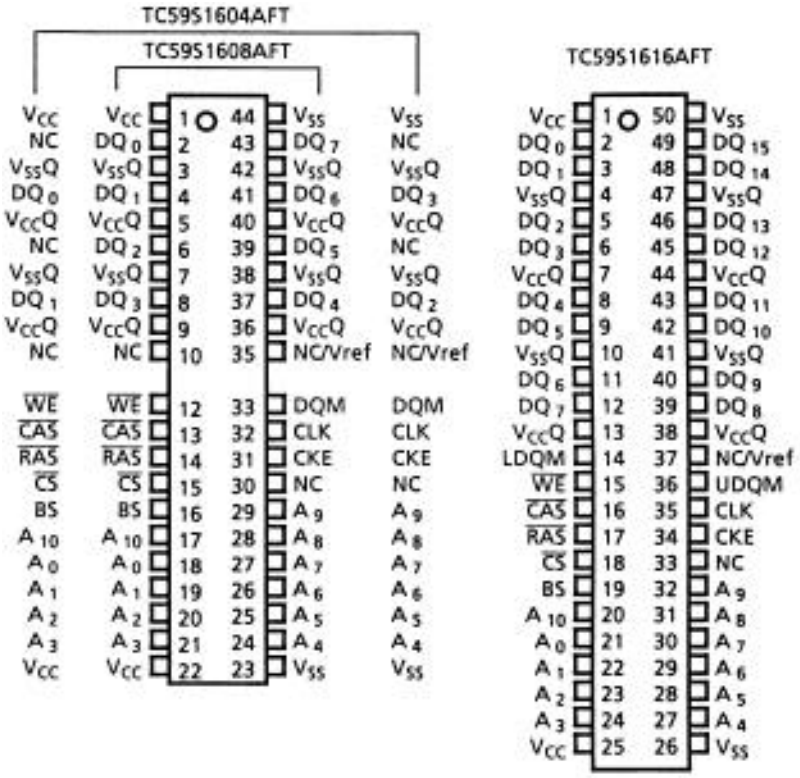
Key Parameters

Item	TC59S1616/1608/1604	
	-10	-12
t_{CK} Clock Cycle Time (Min.)	10ns	12ns
t_{RAS} Active to Precharge Command Period (Min.)	60ns	72ns
t_{CAC} Access Time from Read Command (Max.)	26ns	32ns
t_{AC} CLK Access Time from CLK (Max.)	7.5ns	9ns
t_{RC} Ref/Active to Ref/Active Command Period (Min.)	100ns	120ns
I_{CC1} Operation Current (Max.) (Single bank)	80mA	70mA
I_{CC4} Burst Operation Current (Max.)	120mA	100mA

Pin Name

A0 ~ A10	Address
BS	Bank Select
DQ0 ~ DQ3 (TC59S1604)	Data Input/Output
DQ0 ~ DQ7 (TC59S1608)	
DQ0 ~ DQ15 (TC59S1616)	
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable Input
DQM (TC59S1608/1604)	Output disable/Write Mask
UDQM/LDQM (TC59S1616)	
CLK	Clock inputs
CKE	Clock enable
V_{CC}	Power (+3.3V)
V_{SS}	Ground
$V_{CC}Q$	Power (+3.3V) (for I/O buffer)
$V_{SS}Q$	Ground (for I/O buffer)
NC	No Connection
Vref	Input Reference Voltage

Pin Connection



Absolute Maximum Ratings

Symbol	Characteristic	Rating	Unit	Note
V_{IN}, V_{OUT}	Input, Output Voltage	-0.3 ~ V_{CC} + 0.3	V	1
V_{CC}	Power Supply Voltage	-0.3 ~ 4.6	V	1
T_{OPR}	Operating Temperature	0 ~ 70	°C	1
T_{STG}	Storage Temperature	-55 ~ 150	°C	1
T_{SOLDER}	Soldering Temperature (10s)	260	°C	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

Recommended DC Operating Conditions (Ta = 0 ~ 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	2
$V_{CC}Q$	Power Supply Voltage (for I/O Buffer)	3.0	3.3	3.6	V	2
V_{IH}	LVTTL Input High Voltage	2.0	–	V_{CC} + 0.3	V	2
V_{IL}	LVTTL Input Low Voltage	-0.3	–	0.8	V	2
V_{REF}	Reference Voltage	1.35	1.5	1.65	V	2
V_{IH}	T-LVTTL Input High Voltage	V_{REF} + 0.2	–	V_{CC} + 0.3	V	2
V_{IL}	T-LVTTL Input Low Voltage	-0.3	–	V_{REF} - 0.2	V	2
R_T	T-LVTTL Termination Resistor	–	50	0.8	Ω	

Capacitance (V_{CC} = 3.3V, f = 1MHz, Ta = 25°C)

TC59S1608/1604AFT

Symbol	Parameter	Min.	Max.	Unit
C_I	Input Capacitance (A0 - A10, BS, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, CKE)	–	4	pF
	Input Capacitance (CLK)	–	7	
C_O	Input/Output Capacitance	–	5	

TC59S1616AFT

Symbol	Parameter	Min.	Max.	Unit
C_I	Input Capacitance (A0 - A10, BS, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, CKE)	–	5	pF
	Input Capacitance (CLK)	–	8	
C_O	Input/Output Capacitance	–	6	

Recommended DC Operating Conditions (V_{CC} = 3.3V ±0.3V, Ta = 0 ~ 70°C)

Item			Symbol	-10		-12		Unit	Note
				Min.	Max.	Min.	Max.		
Operating Current t_{CK} = min, t_{RC} = min Active-Precharge command cycling Without Burst Operation	1 bank operation		I_{CC1}		80		70	mA	3
	2 bank interleave operation		I_{CC1B}		140		130		3
Standby Current t_{CK} = min, $\overline{CS}$ = V_{IH} $V_{IH/IL}$ = $V_{IH\ (min)}$/ $V_{IL\ (max)}$ bank: inactive state	CKE = V_{IH}		I_{CC2}		25		22		3
	CKE = V_{IL} (Power Down Mode)		I_{CC2P}		2		2		3
Standby Current CLK = V_{IL} = min, $\overline{CS}$ = V_{IH} $V_{IH/IL}$ = $V_{IH\ (min)}$/ $V_{IL\ (max)}$ bank: inactive state	CKE = V_{IH}		I_{CC2S}		3		3		
	CKE = V_{IL} (Power Down Mode)	Low Power Version (AFTL/ASTL)	I_{CC2PS}		1		1		
		Standard Products (AFT/AST)			2		2		
No Operating Current t_{CK} = min $\overline{CS}$ = $V_{IH\ (min)}$ bank: inactive state (2 bank)			I_{CC3}		25		22		3,4
Burst Operating Current $\overline{CS}$ = $V_{IH\ (min)}$ Read/Write command cycling			I_{CC4}		120		100		3,4
Auto Refresh Current t_{CK} = min Auto Refresh command cycling			I_{CC5}		80		70		3
Self Refresh Current Self Refresh mode CKE = 0.2V	Low Power Version (AFTL/ASTL)		I_{CC6}		200		200	µA	
	Standard Products (AFT/AST)				1		1	mA	

Item	Symbol	Min.	Max.	Unit	Note
Input Leakage Current (0V≤V_{IN}≤V_{CC} All other pins not under test = 0V)	$I_{I(L)}$	-5	5	µA	
Output Leakage Current (Output disable, 0V≤V_{IN}≤V_{CCQ})	$I_{O(L)}$	-5	5	µA	
LVTTL Output “H” Level Voltage (I_{OUT} = -2mA)	V_{OH}	2.4	–	V	
LVTTL Output “L” Level Voltage (I_{OUT} = 2mA)	V_{OL}	–	0.4	V	
T - LVTTL Output “H” Level Voltage (I_{OUT} = -2mA)	V_{OH}	V_{REF} + 0.4	–	V	
T - LVTTL Output “L” Level Voltage (I_{OUT} = 2mA)	V_{OL}	–	V_{REF} + 0.4	V	

Electrical Characteristics and Recommended AC Operating Conditions (V_{CC} = 3.3V ± 0.3V, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

Symbol	Parameter		-10		-12		Unit	Note
			Min.	Max.	Min.	Max.		
t_{RC}	Ref/Active to Ref/Active Command Period		100		120		ns	9
t_{RAS}	Active to Precharge Command Period		60	100000	72	100000		9
t_{RCD}	Active to Read/Write Command Delay Time (Write)		20		24			9, 10
t_{RCD}	Active to Read/Write Command Delay Time (Read)		30		36			9, 10
t_{CCD}	Read/Write (a) to Read/Write (b) Command Delay Time (Read)		1		1		cycle	9, 10
t_{RP}	Precharge to Active Command Period		30		36		ns	9
t_{RRD}	Active (a) to Active (b) Command Period		20		24			9
t_{CAC}	Access Time from Read Command			26		32		9
t_{WR}	Write Recovery Time	CL * = 1	30		36		ns	
		CL * = 2	15		18			
		CL * = 3	1CLK + 10		1CLK + 12			
t_{CK}	CLK Cycle Time	CL * = 1	30	1000	36			
		CL * = 2	15	1000	18			
		CL * = 3	10	1000	12			
t_{CH}	CLK High Level Width		3		4			11
t_{CL}	CLK Low Level Width		3		4			11
t_{AC}	Access Time from CLK	CL * = 1		26		32		
		CL * = 2		11		14		
		CL * = 3		7.5		9		
t_{OH}	Output Data Hold Time		3		3			
t_{HZ}	Output Data High Impedance Time		2		2			8
t_{LZ}	Output Data Low Impedance Time		0		0			
t_{SB}	Power Down Mode Entry Time		0		0			
t_T	Transition Time of CLK (Rise and Fall)		1		1			
t_{DS}	Data-in Set-up Time		3		3.5			
t_{DH}	Data-in Hold Time		1		1.5			
t_{AS}	Address Set-up Time		3		3.5			
t_{AH}	Address Hold Time		1		1.5			
t_{CKS}	CKE Set-up Time		3		3.5			
t_{CKH}	CKE Hold Time		1		1.5			
t_{CMS}	Command Set-up Time		3		3.5			
t_{CMH}	Command Hold Time		1		1.5			
t_{REF}	Refresh Time			64			ms	
t_{RSC}	Mode Register Set Cycle Time		20		0		ns	9

* CL is $\overline{CAS}$ Latency.

NOTE:

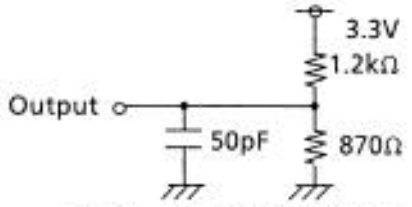
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depends on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. Power-up sequence is described in NOTE 12.
6. AC test conditions

LVTTL Interface

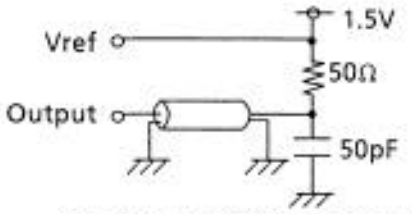
Reference Level of Output Signals	1.4V/1.4V
Output Load	Reference to the Under Output Load (B)
Input Signal Levels	2.4V/0.4V
Transition Time (Rise and Fall) of Input Signals	2ns
Reference Level of Input Signals	1.4V

Terminated LVTTL Interface

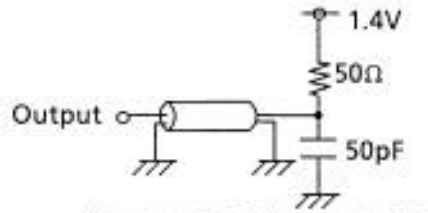
Reference Level of Output Signals	1.5V/1.5V
Output Load	Reference to the Under Output Load
Input Signal Levels	V_{REF} + 0.4/V_{REF} - 0.4
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	1.5V



LVTTL A.C. TEST LOAD (A)



Terminated LVTTL A.C. TEST LOAD



LVTTL A.C. TEST LOAD (B)

7. Transition times are measured between V_{IH} and V_{IL}. Transition (rise and fall) of input signals are fixed slope.
8 t_{HZ} defines the time at which the outputs achieve the open circuit condition and are not reference levels.
9. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows:

   the number of clock cycles = specified value of timing/clock period (count fractions as a whole number).

Latency relationship to frequency (Unit: clock cycles)

-10 Version (calculation with t_{CK} = 10ns ~ 30ns)

CLK period (t_{PRD})	t_{RC}	t_{RAS}	t_{RF}	t_{CAC}	$t_{RCD\ (R)}$	$t_{RCD\ (W)}$	t_{RSC}	t_{RRD}
	100ns	**60ns**	**30ns**	**26ns**	**30ns**	**20ns**	**20ns**	**20ns**
≥30.0ns	4	2	1	1	1	1	1	1
≥20.0ns	5	3	2	2	2	1	1	1
≥18.0ns	7	4	2	2	2	2	2	2
≥15.0ns	8	4	2	2	2	2	2	2
≥13.4ns	9	5	3	2	3	2	2	2
≥12.5ns	10	5	3	3	3	2	2	2
≥12.0ns	10	5	3	3	3	2	2	2
≥10.0ns	10	6	3	3	3	2	2	2

-12 Version (calculation with t_{CK} = 12ns ~ 36ns)

CLK period (t_{PRD})	t_{RC}	t_{RAS}	t_{RF}	t_{CAC}	$t_{RCD\ (R)}$	$t_{RCD\ (W)}$	t_{RSC}	t_{RRD}
	120ns	**72ns**	**36ns**	**32ns**	**36ns**	**24ns**	**24ns**	**24ns**
≥36.0ns	4	2	1	2	3	3	2	1
≥24.0ns	5	3	2	2	4	4	3	2
≥20.0ns	6	3	2	3	5	5	3	2
≥18.0ns	7	4	2	3	5	5	4	2
≥16.0ns	8	4	2	3	6	6	4	2
≥15.0ns	8	5	1	2	3	3	2	1
≥14.4ns	9	5	2	2	4	4	3	2
≥13.4ns	9	6	2	3	5	5	3	2
≥12.0ns	10	6	2	3	6	6	4	2

10. The minimum delay time from Active to Read command is different from that of the Write command.
11. t_{CH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min.). t_{CL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max.).
12. Power Up Sequence

    Power up must be performed in the following sequence.

    (1) Power must be applied to V_{CC} and $V_{CC}Q$ (simultaneously) when all input signals are held “NOP” state. The CLK signals must be started at the same time.

    During V_{CC} ramping up to the valid level, DQM and CKE should be the same as V_{CC} to ensure output Hi-z.

    (2) After power-up a pause of 200μseconds minimum is required. Then, it is recommended that DQM signal is held “high” (V_{CC} levels) to ensure DQ output to be in the high impedance.

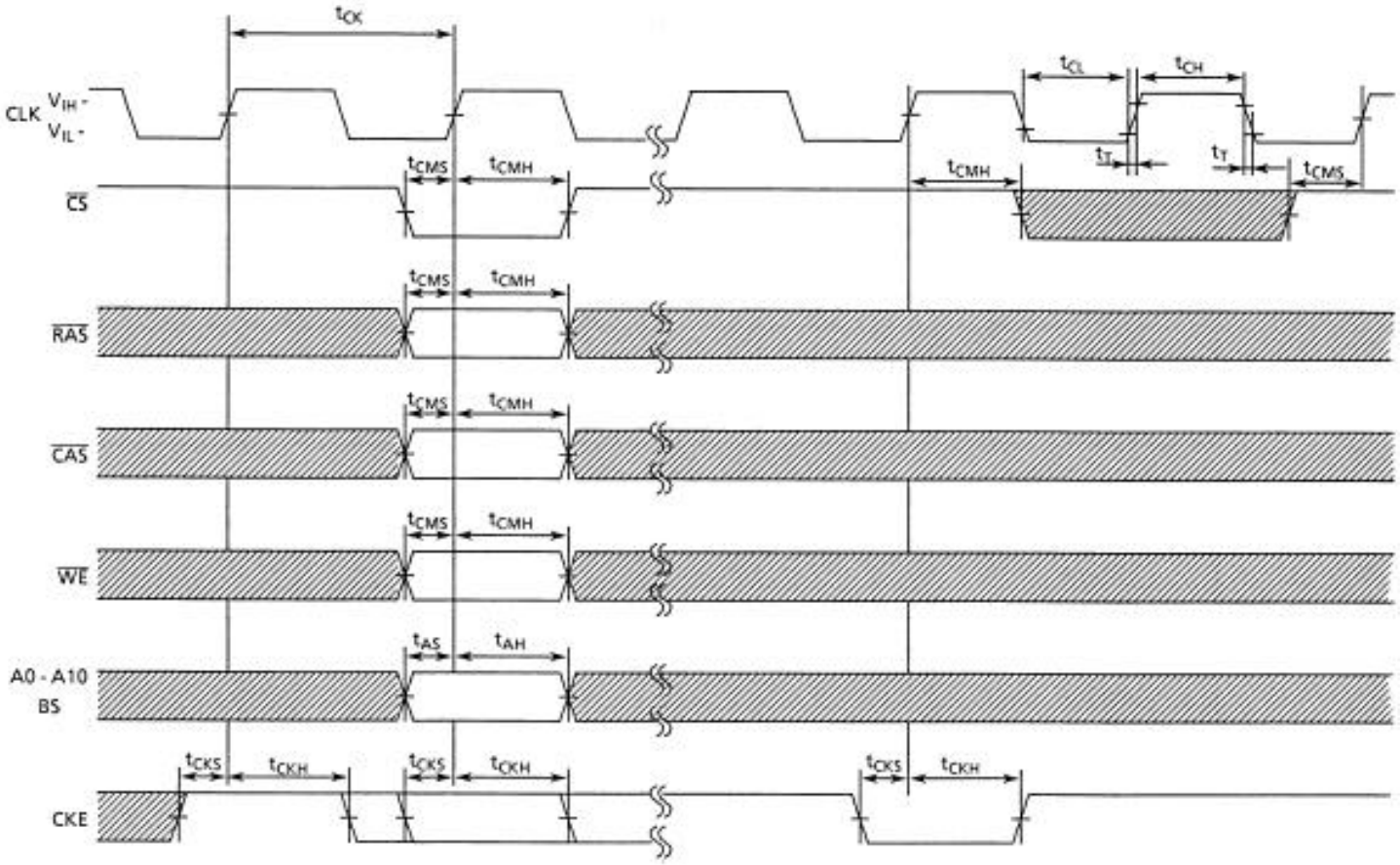
    (3) Both banks must be precharged.

    (4) Mode register set command must be asserted to initialize the Mode register.

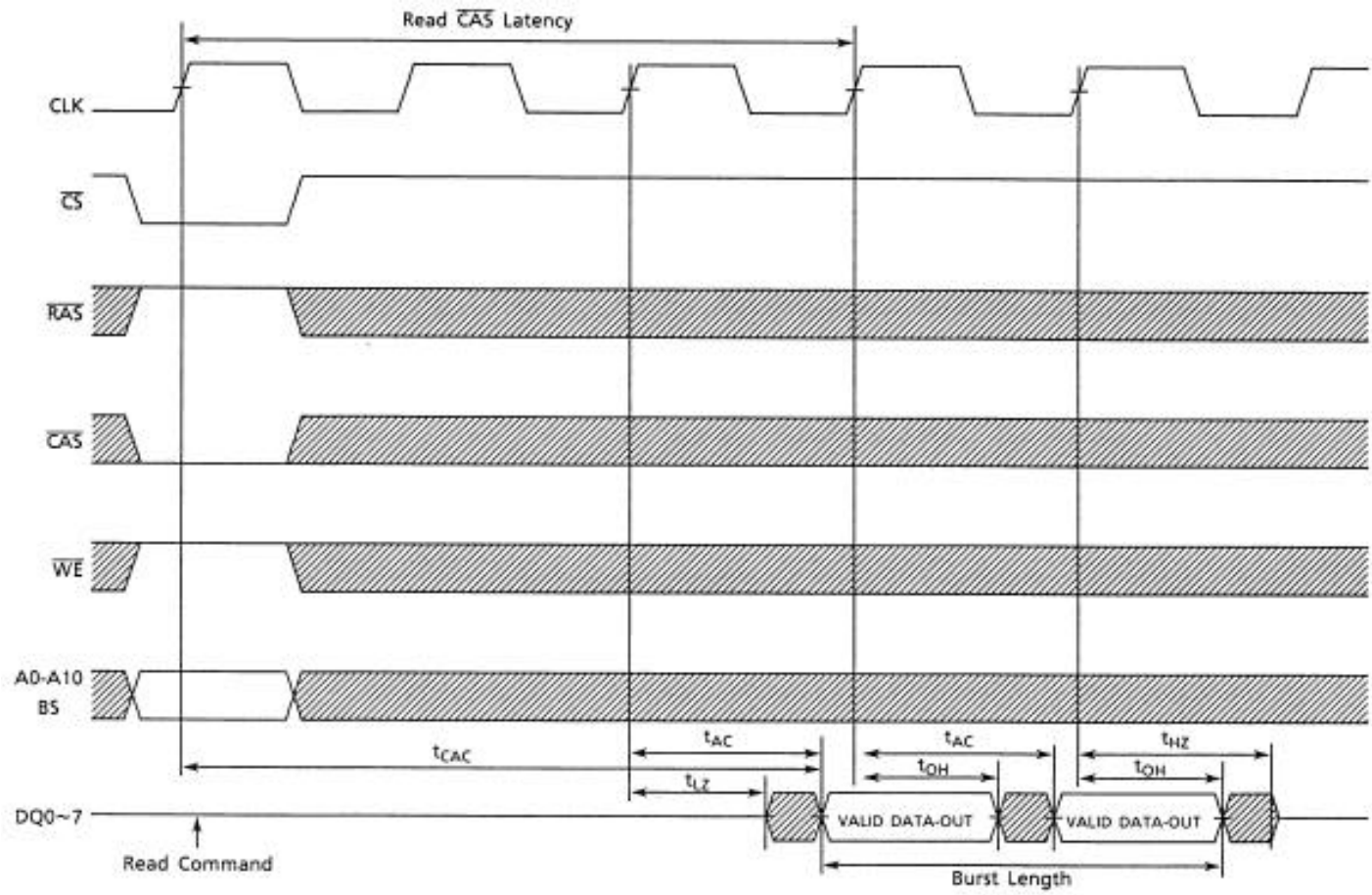
    (5) A minimum of 8 AutoRefresh dummy cycles must be required to stabilize the internal circuity of the device.

Timing Waveform

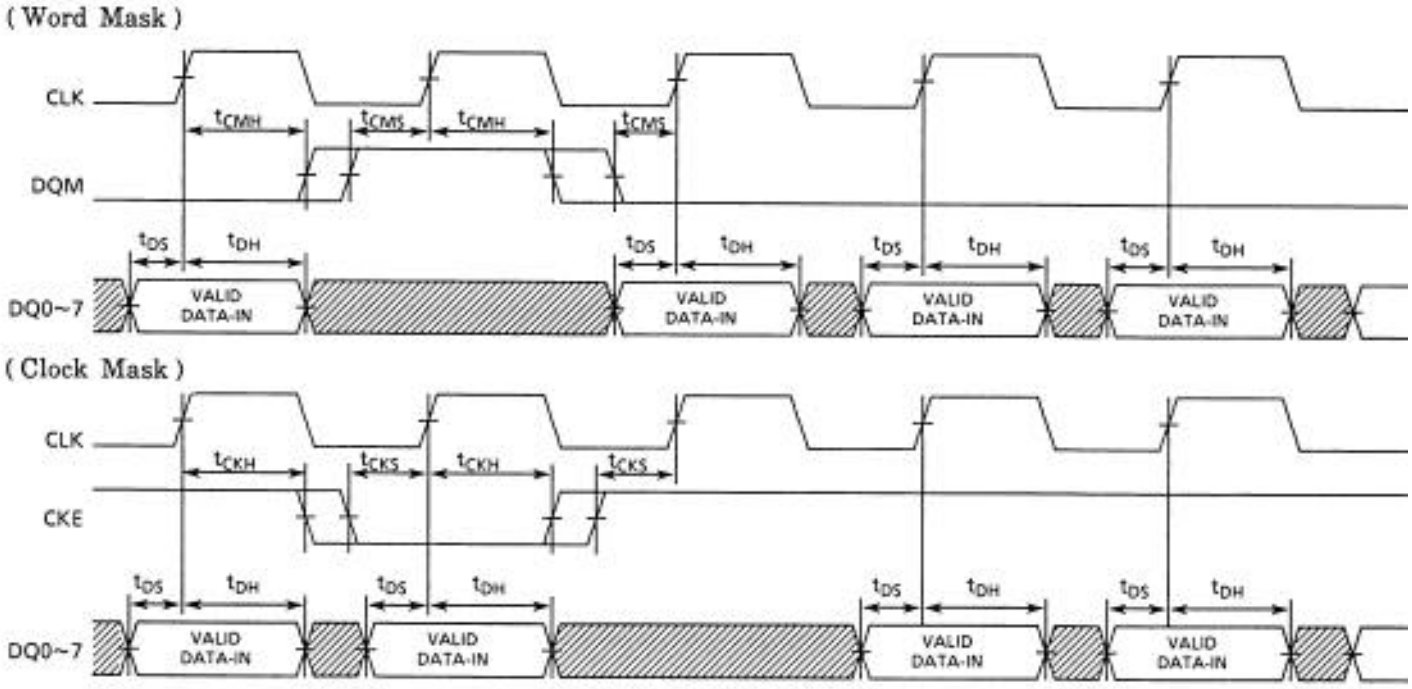
Command Input Timing



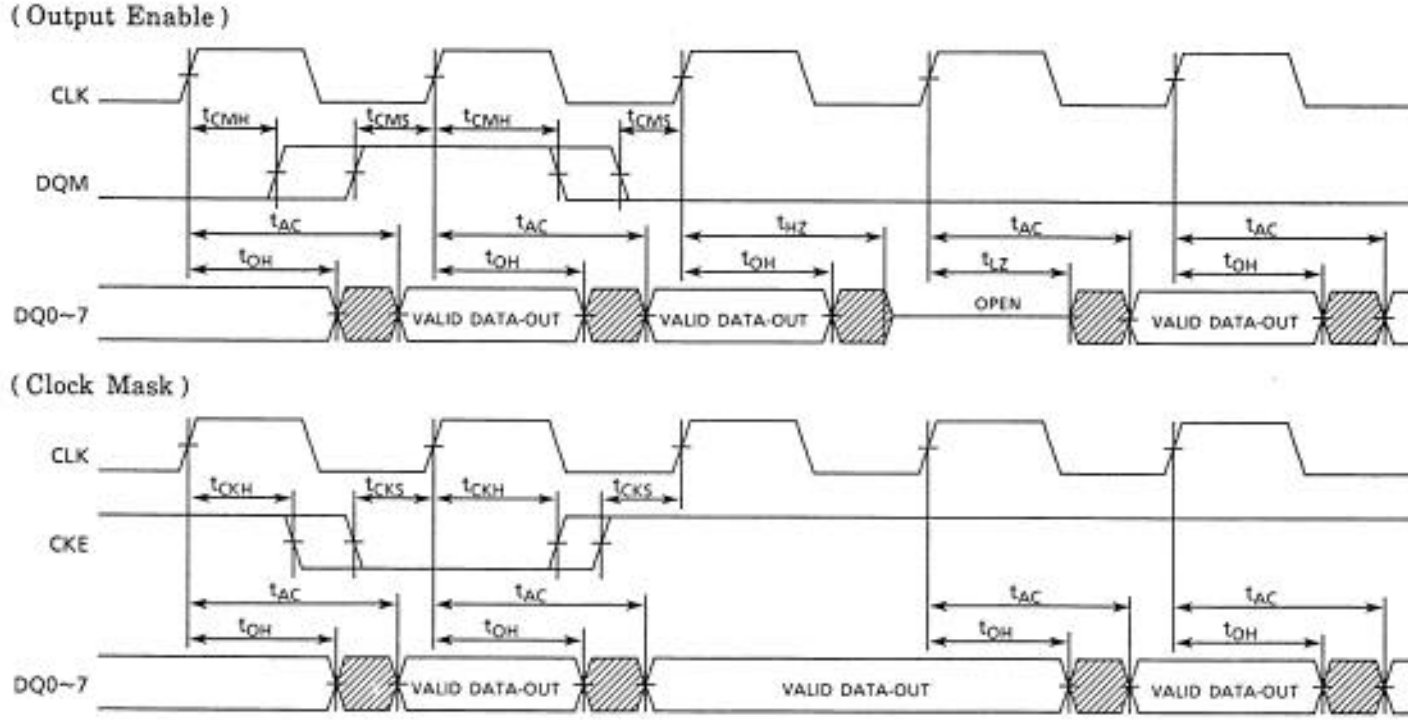
Read Timing


Read CAS Latency
CLK
CS
RAS
CAS
WE
A0-A10
BS
tCAC
tAC
tLZ
tAC
tOH
tHZ
tOH
DQ0~7
VALID DATA-OUT
VALID DATA-OUT
Read Command
Burst Length

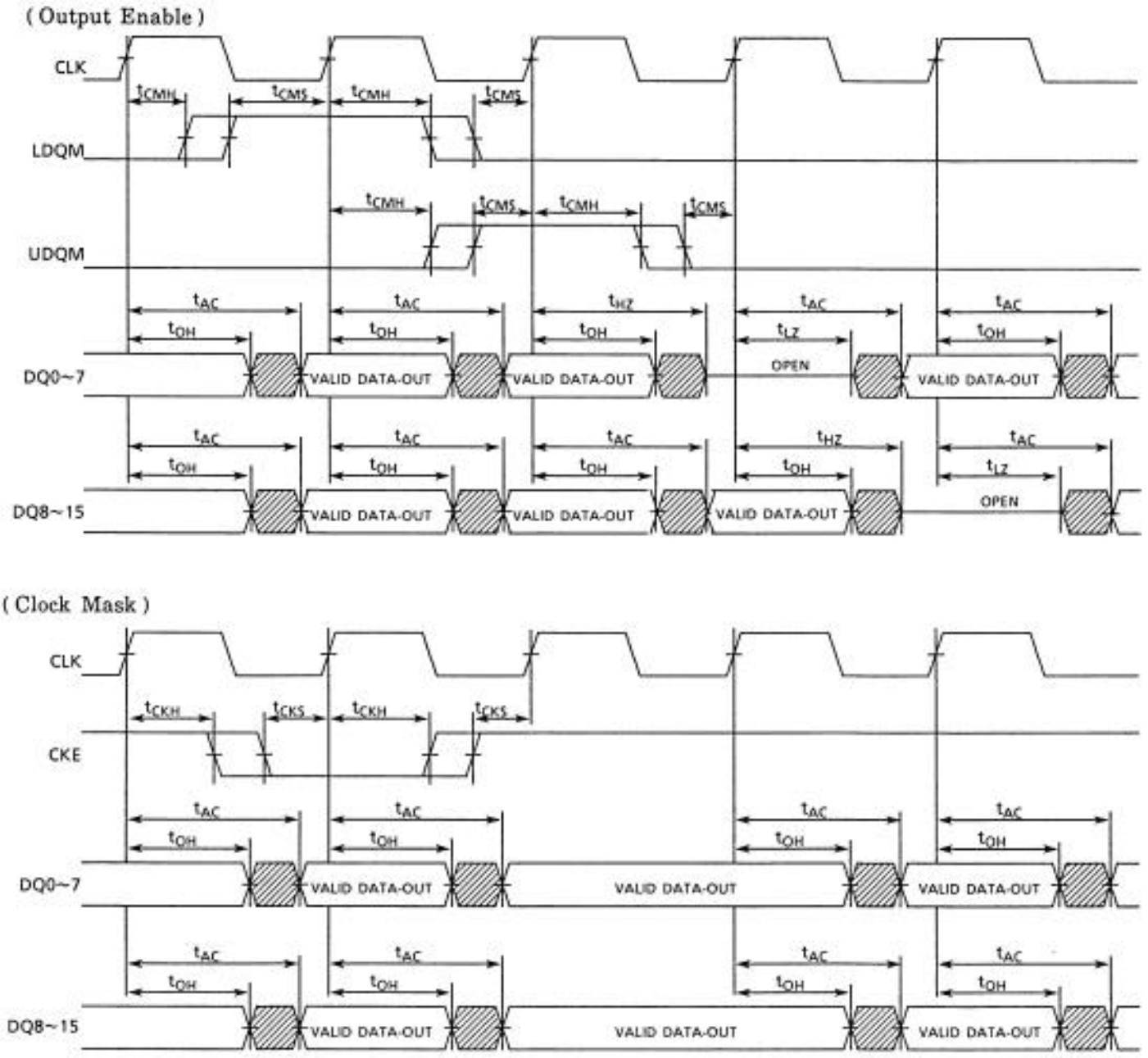
Control Timing of Input Data (TC59S1608/1604AFT)



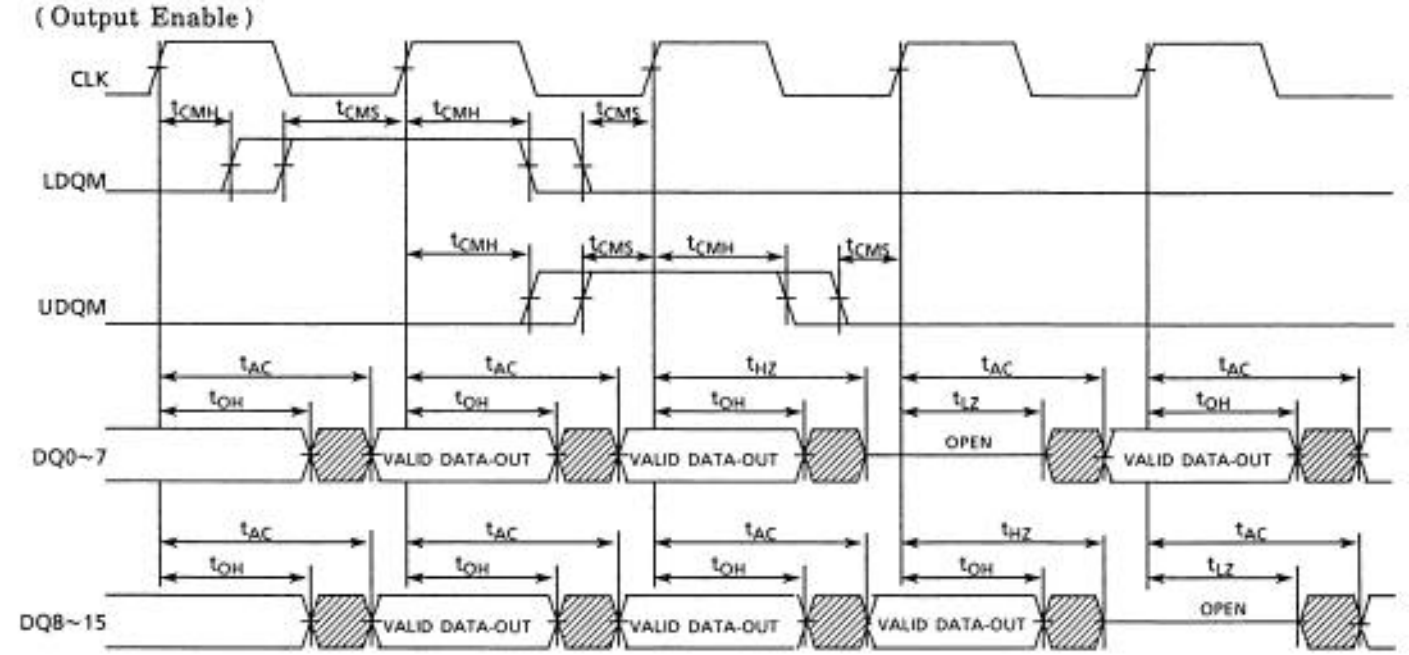
Control Timing of Output Data (TC59S1608/1604AFT)



Control Timing of Input Data (TC59S1616AFT)



Control Timing of Output Data (TC59S1616AFT)



Mode Register Set Cycle

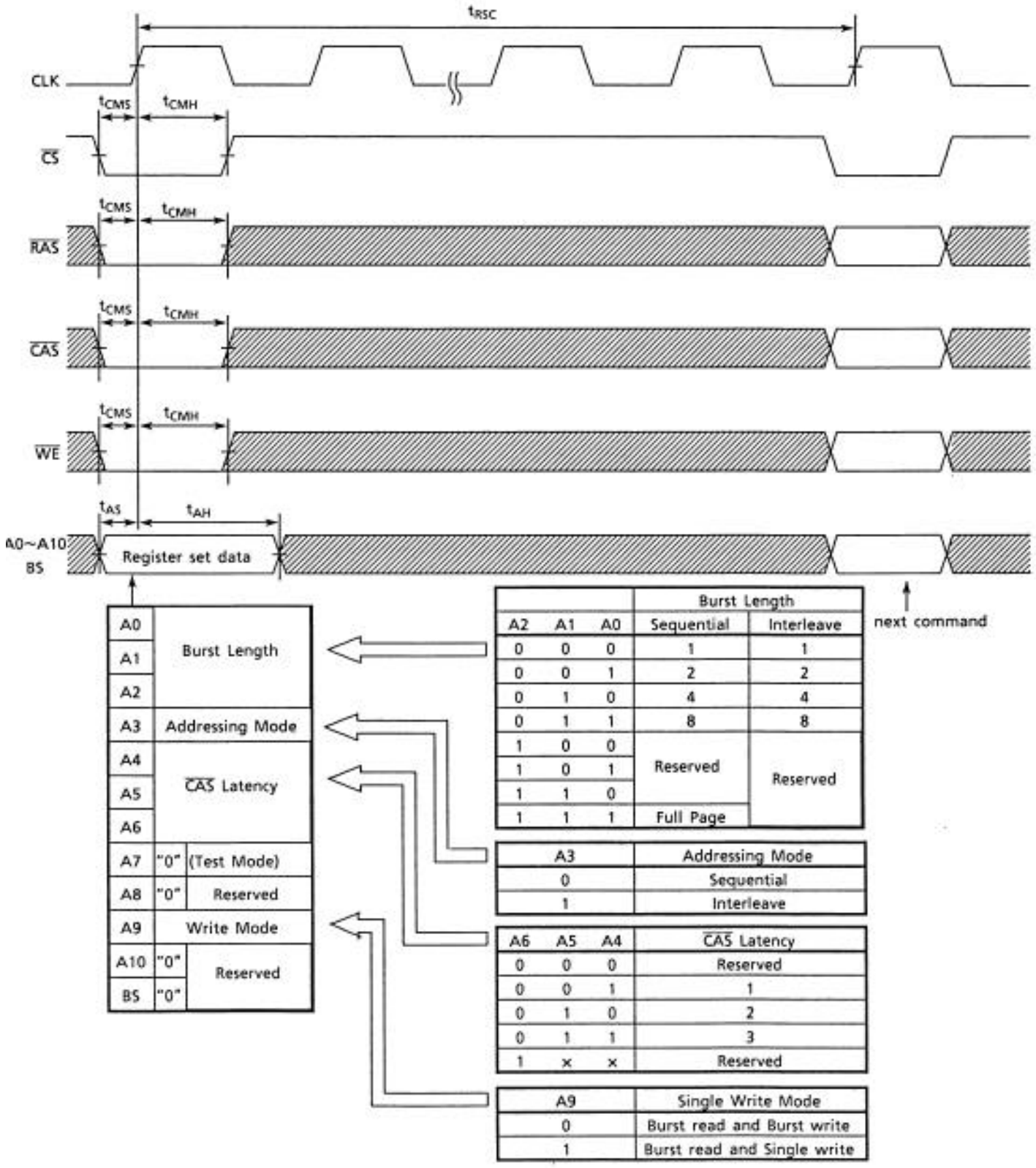


Figure 2. Interleaved Bank Read (Burst Length = 4, CAS Latency = 3, Autoprecharge)